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(11)出願人 000005109

株式会社日立製作所

東京都千代田区神田区西千代田6番地

(11)出願人 000233169

株式会社日立マイコンシステム

東京都小平市上水本町5丁目22番1号

(12)発明者 金本 光一

東京都小平市上水本町5丁目20番1号

株式会社日立製作所 半導体事業部内

(12)発明者 西田 隆文

東京都小平市上水本町5丁目22番1号

株式会社日立マイコンシステム内

(14)代理人 弁護士 森田 敬吾

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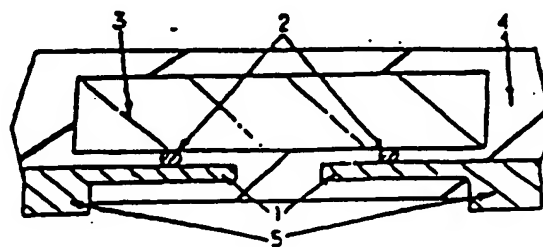
(54)【発明の名称】半導体装置

(57)【要約】

【目的】 半導体装置の高圧電圧における実効寿命を向上すること。

【構成】 半導体チップとそれに電気的に接続された内部リードを絶縁で封止した半導体装置であって、前記半導体装置の封止部材の底部もしくは、上部から内部リードの一部を突出させる。

図1



(10021) として、図2-54に示した断面形状から算出する断面モーメントは、断面に開口がある

される。

【0022】これにより、図4、図5に示した4の位置から突出していた外部リードの分だけ、又はスペースを切り取るなり、他の位置等の突起に切り替へたりすることが可能になる。

【0023】次に、図5を用いて、本発明の半導体装置のリードフレームについて説明する。

【0024】図5において、3Aは大型の半導体チップ、3Bは小型の半導体チップ、2Aは大型の半導体チップと内部リード部分を搭載するパンプ、2Bは大型の半導体チップと内部リード部分を搭載するパンプをそれぞれ示す。

【0025】図5に示すように、本発明の半導体装置のリードフレームの形状は、フレームの中心付近から内部リードが放射状に広がっている。

【0026】これにより、従来で用いた異なるサイズの半導体チップである大型の半導体チップ3Aを搭載する場合でも、小型の半導体チップ3Bを搭載する場合でも、各半導体チップ3A、3Bのバンド位置を内部リード1上の搭載可能位置に一致し、その位置にパンプ2A、2Bを設けることで半導体チップ3A、3Bと内部リード部分1とを接続できる。このパンプを用いる内部リードと半導体チップとの電気的な接続はワイヤ接続では得られない有用な手段である。

【0027】すなわち、本発明のリードフレーム一つで多数の半導体チップを適用できる。

【0028】次に、本発明の他の実施例を図6と図7に示す。

【0029】図6に示す半導体装置の例は、図1の例1に示した半導体装置の内部リード部分1と外部リード部分の機能をなくしたものであり、内部リードと外部リードを共用化したリードを設けてある。すなわち、本実施例によれば、リードの幅のほぼ2/3がレジスタにより埋め込まれ、その埋め込まれたリード一面（上面）が半導体チップとの電気的接続部をなし、一方、リードの幅のほぼ1/3がレジスタから突出、その突出した側面は基板裏面への接続端子、つまり外部リードとなる。

【0030】これにより、基板内における基板と外部リードの接続部分の面積を減らすとともに、形状化パッケージが得られる。リードフレームに突起をつけなくともよくなる。

【0031】図7に示す半導体装置の例は、前述の例1に示した半導体装置の半導体チップ3上に熱伝導フィン6を設け、半導体チップから発生する熱を逃がしてやるものである。

【0032】なお、本実施例は多角形型の半導体装置をそれぞれ取り替へたが正方形型の半導体装置についても

同様である。

【0033】また、本実施例のCOL (CHIP ON LEAD) 構造の半導体装置は、基板から外部リードを突出させた例を取り替へたが、LOC (LEAD ON CHIP) 構造の半導体装置においては、上面から外部リードを突出させる。

【0034】したがって、半導体チップとそれと電気的に接続された内部リードを基板で封止した半導体装置であって、上記半導体装置の封止部材の底面もしくは、上面から内部リードの一部を突出させることにより、半導体装置の封止部材の占める面積内に外部リードが収まり、従来の外部リードの突出によって余分とられていた面積面積を減小して得るもので、半導体装置の基板裏面における突起部を向上することが可能となる。

【0035】以上、本発明者によってなされた発明を、図1～図7に示す実施例に基づいて説明したが、本発明は、図1～図7に示す実施例のものではなく、その要旨を逸脱しない範囲において種々変更可能であることは勿論である。

【0036】

【発明の効果】本発明において説明される発明のうち代表的なものによって得られる効果を簡単に説明すれば、下記のとおりである。

【0037】半導体チップとそれと電気的に接続された内部リードを基板で封止した半導体装置であって、上記半導体装置の封止部材の底面もしくは、上面から内部リードの一部を突出させることにより、半導体装置の封止部材の占める面積内に外部リードが収まり、従来の外部リードの突出によって余分とられていた面積面積を減小して得るもので、半導体装置の基板裏面における突起部を向上することが可能となる。

【図面の簡単な説明】

【図1】本発明の一実施例である半導体装置の構造を説明するための図である。

【図2】本実施例の半導体装置の側面図である。

【図3】本実施例の半導体装置の俯視図である。

【図4】本実施例の半導体装置の底面からみた平面図である。

【図5】本実施例の半導体装置におけるリードフレームの構造を説明するための図である。

【図6】本発明の他の実施例である半導体装置の構造を説明するための図である。

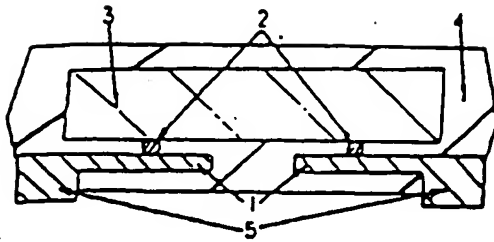
【図7】本発明の他の実施例である半導体装置の構造を説明するための図である。

【符号の説明】

1…内部リード部分、2…パンプ、3…チップ、4…封止部材、5…外部リード部分、6…熱伝導フィン。

(B1)

图 1



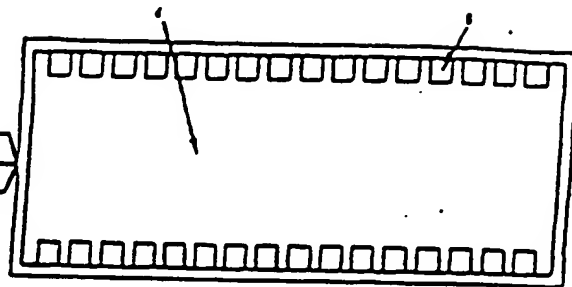
(B2)

图 2



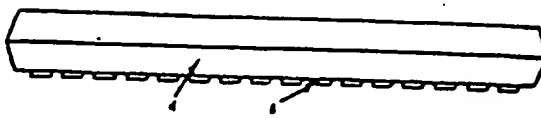
(B4)

图 4



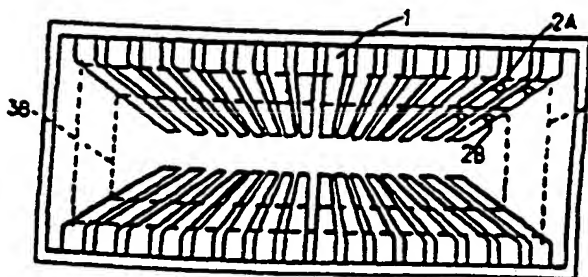
(B3)

图 3



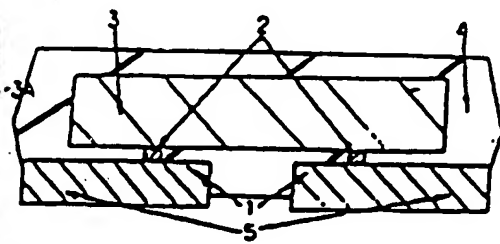
(B5)

图 5



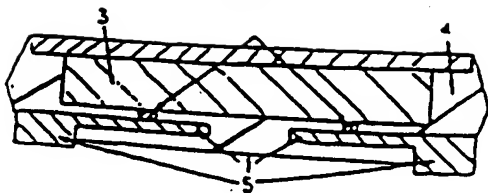
(B6)

图 6



(B7)

图 7



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(12) 発明者 角谷 征樹

東京都小平市上木本町5丁目20番1号

株式会社日立製作所半導体事業部内

[TITLE OF THE INVENTION]

Semiconductor Device

5

[CLAIMS]

1. A semiconductor device including a semiconductor chip, inner leads electrically connected to the semiconductor chip, and a resin encapsulate adapted to encapsulate the semiconductor chip and the inner leads, wherein each of the inner leads is partially protruded from a lower surface or an upper surface of the resin encapsulate.

15

2. The semiconductor device in accordance with claim 1, wherein the inner leads are electrically connected to the semiconductor chip by bumps, respectively.

20

3. A semiconductor device including a semiconductor chip, a plurality of inner leads electrically connected to the semiconductor chip, and a resin encapsulate adapted to encapsulate the semiconductor chip and the inner leads, wherein each of the inner leads is encapsulated at a portion of the thickness thereof while being exposed at the remaining portion thereof in such a fashion that it has an

25

encapsulated main lead surface serving as an electrical connection to the semiconductor chip, and an exposed main lead surface positioned opposite to the encapsulated main lead surface, the exposed main lead surface serving as an outer lead.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a technique effective if applied to semiconductor devices.

[DESCRIPTION OF THE PRIOR ART]

In conventional semiconductor devices, a semiconductor chip is typically connected with inner leads by means of wires or bumps. Such a semiconductor device has a structure in which outer leads are laterally protruded from an encapsulate.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

After reviewing the prior art, the inventors have found the following problems. A down-sizing of recent system appliances using semiconductor devices has resulted in a requirement to reduce the size of circuit boards on which semiconductor devices are mounted. To this end, attempts to reduce the size of semiconductor devices have

been made in order to achieve an improvement in the mounting efficiency of circuit boards resulting in a reduction in the size of those circuit boards.

5 In most cases, such a reduction in the size of semiconductor devices have been achieved by reducing the size of semiconductor chips. For such a reduction in the size of semiconductor devices, outer leads have not been the subject of interest. That is, there has been no attempt to reduce the area occupied by outer leads of a semiconductor device on a circuit board. Since 10 conventional semiconductor devices have a structure in which outer leads are laterally protruded from a resin encapsulate, they have a mounting area increased by the area of the outer leads laterally protruded from the resin encapsulate. As a result, the conventional semiconductor 15 devices involve a problem in that the mounting efficiency thereof on a circuit board is degraded.

An object of the invention is to provide a technique capable of improving the mounting efficiency of a semiconductor device on a circuit board. 20

Other objects and novel features of the present invention will become more apparent after a reading of the following detailed description when taken in conjunction with the drawings.

25

[MEANS FOR SOLVING THE SUBJECT MATTERS]

A representative of inventions disclosed in this application will now be summarized in brief.

30 In a semiconductor device in which a semiconductor chip and inner leads electrically connected to the semiconductor chip are encapsulated by resin, each of the

inner leads is partially protruded from a lower surface or an upper surface of the resin encapsulate.

5 For a semiconductor device in which a semiconductor chip and inner leads electrically connected to the semiconductor chip are encapsulated by resin, the present invention can improve the mounting efficiency of the semiconductor device on a circuit board by protruding a portion of each inner lead from the lower or upper surface of the resin encapsulate in such a fashion that the outer leads of the semiconductor device are received in an area occupied by the resin encapsulate, thereby reducing the mounting area of the outer leads by the area of outer leads laterally protruded from a resin encapsulate in the case of conventional semiconductor devices.

10
15 Now, the present invention will be described in detail in conjunction with embodiments thereof.

In the drawings associated with the embodiments, elements having the same function are denoted by the same reference numeral, and repeated description thereof will be omitted.

[EMBODIMENTS]

Fig. 1 is a view illustrating a semiconductor device having a structure according to an embodiment of the present invention. The semiconductor device according to the embodiment of the present invention shown in Fig. 1 has a rectangular structure. Fig. 2 is a side view of the semiconductor device when viewed at the shorter side of the rectangular structure. Fig. 3 is a side view of the semiconductor device when viewed at the longer side of the rectangular structure. Fig. 4 is a plan view of the semiconductor device when viewed at the bottom.

In Figs. 1 to 4, the reference numeral 1 denotes

inner lead portions, 2 bumps, 3 a chip, 4 a resin encapsulate, and 5 outer lead portions, respectively.

As shown in Fig. 1, the semiconductor device of the present embodiment includes leads having a stepped lead structure. Each lead has an inner lead portion 1 serving as an inner lead, and an outer lead portion 5 serving as an outer lead.

The stepped lead structure can be obtained by half-etching the inner lead portions 1 of the leads. Alternatively, the stepped lead structure may be obtained by bonding two lead sheets to each other in such a fashion that they define a step therebetween, and then cutting the bonded lead sheets.

Within the resin encapsulate 4, bumps 2, which may be made of, for example, solder, are provided on the inner lead portions 1, respectively. Through these bumps 2, the inner lead portions are electrically connected to the semiconductor chip 3. Bumps previously provided at the semiconductor chip 3 may also be used as means for electrically connecting the inner lead portions 1 to the semiconductor chip 3. Alternatively, wires may be used.

As shown in Figs. 2 to 4, the outer lead portions 5, which are protruded from the resin encapsulate 4, are mounted on a circuit board or the like while being in surface contact with the circuit board. Accordingly, it is

possible to reduce the mounting space of the semiconductor device by the area of outer leads laterally protruded from a resin encapsulate in the case of conventional semiconductor devices. Otherwise, this area may be used to
5 mount other elements.

Now, a lead frame included in the semiconductor device according to the present embodiment will be described in conjunction with Fig. 5.

In Fig. 5, the reference numeral 3A denotes a larger
10 semiconductor chip, 3B a smaller semiconductor chip, 2A bumps for coupling inner leads to the larger semiconductor chip, and 2B bumps for coupling the inner leads to the smaller semiconductor chip, respectively.

As shown in Fig. 5, the lead frame of the
15 semiconductor device according to the present embodiment has a structure in which inner leads extend radially around an area near the center of the lead frame. Accordingly, any one of the semiconductor chips having different sizes, that is, the larger semiconductor chip 3A and smaller
20 semiconductor chip 3B indicated by phantom lines, can be connected with the inner lead portions 1 by shifting each pad position of the semiconductor chip 3A or 3B to a position where the semiconductor chip 3A or 3B can be connected to the inner leads 1, and providing a bump 2A or
25 2B at the shifted position. The electrical connection

between the inner leads and the semiconductor chip obtained by use of bumps as mentioned above provides an useful effect which cannot be expected in the case using wire connection. That is, one lead frame, which is configured in accordance with the present embodiment, can be applied to a variety of semiconductor chips.

Referring to Figs. 6 and 7, other embodiments of the present invention are illustrated, respectively.

In a semiconductor device according to the embodiment of Fig. 6, there is no step between the inner and outer lead portions 1 and 5 of each lead, as compared to the semiconductor device of Fig. 1. In this case, the semiconductor device includes leads each serving as both the inner and outer leads. In accordance with this embodiment, about $2/3$ of the thickness of each lead is encapsulated by resin. One main surface of each lead, namely, the encapsulated main surface (upper surface), serves as an electrical connection to the semiconductor chip. About $1/3$ of the thickness of each lead is exposed from the resin. The other main surface of each lead, namely, the exposed main surface, serves as a connection terminal to a mounting circuit board, for example, an outer lead.

In accordance with such a structure, it is possible to secure the area, where the outer leads can be connected

to the circuit board, upon the mounting of the semiconductor device. Furthermore, a thin package can be produced. In accordance with this embodiment, it is also unnecessary to provide a stepped lead structure for the lead frame.

In a semiconductor device according to the embodiment of Fig. 7, radiation fins 6 are provided on the semiconductor chip 3 shown in Fig. 1 in order to radiate heat generated from the semiconductor chip 3.

Although the above embodiments have been described as being applied to rectangular semiconductor devices, they may also be applied to square semiconductor devices. Also, the above embodiments have been described as being applied to a semiconductor device having a COL (Chip On Lead) structure to protrude outer leads thereof from the lower surface of the encapsulate. In the case of a semiconductor device having an LOC (Lead On Chip) structure, outer leads thereof are protruded from the upper surface of the encapsulate.

For a semiconductor device in which a semiconductor chip and inner leads electrically connected to the semiconductor chip are encapsulated by resin, the present invention can improve the mounting efficiency of the semiconductor device on a circuit board by protruding a portion of each inner lead from the lower or upper surface

of the resin encapsulate in such a fashion that the outer leads of the semiconductor device are received in an area occupied by the resin encapsulate, thereby reducing the mounting area of the outer leads by the area of outer leads laterally protruded from a resin encapsulate in the case of conventional semiconductor devices.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

[EFFECTS OF THE INVENTION]

Effects obtained by a representative one of the inventions disclosed in this application will now be described in brief.

For a semiconductor device in which a semiconductor chip and inner leads electrically connected to the semiconductor chip are encapsulated by resin, the present invention can improve the mounting efficiency of the semiconductor device on a circuit board by protruding a portion of each inner lead from the lower or upper surface of the resin encapsulate in such a fashion that the outer leads of the semiconductor device are received in an area occupied by the resin encapsulate, thereby reducing the mounting area of the outer leads by the area of outer leads laterally protruded from a resin encapsulate in the case of conventional semiconductor devices.